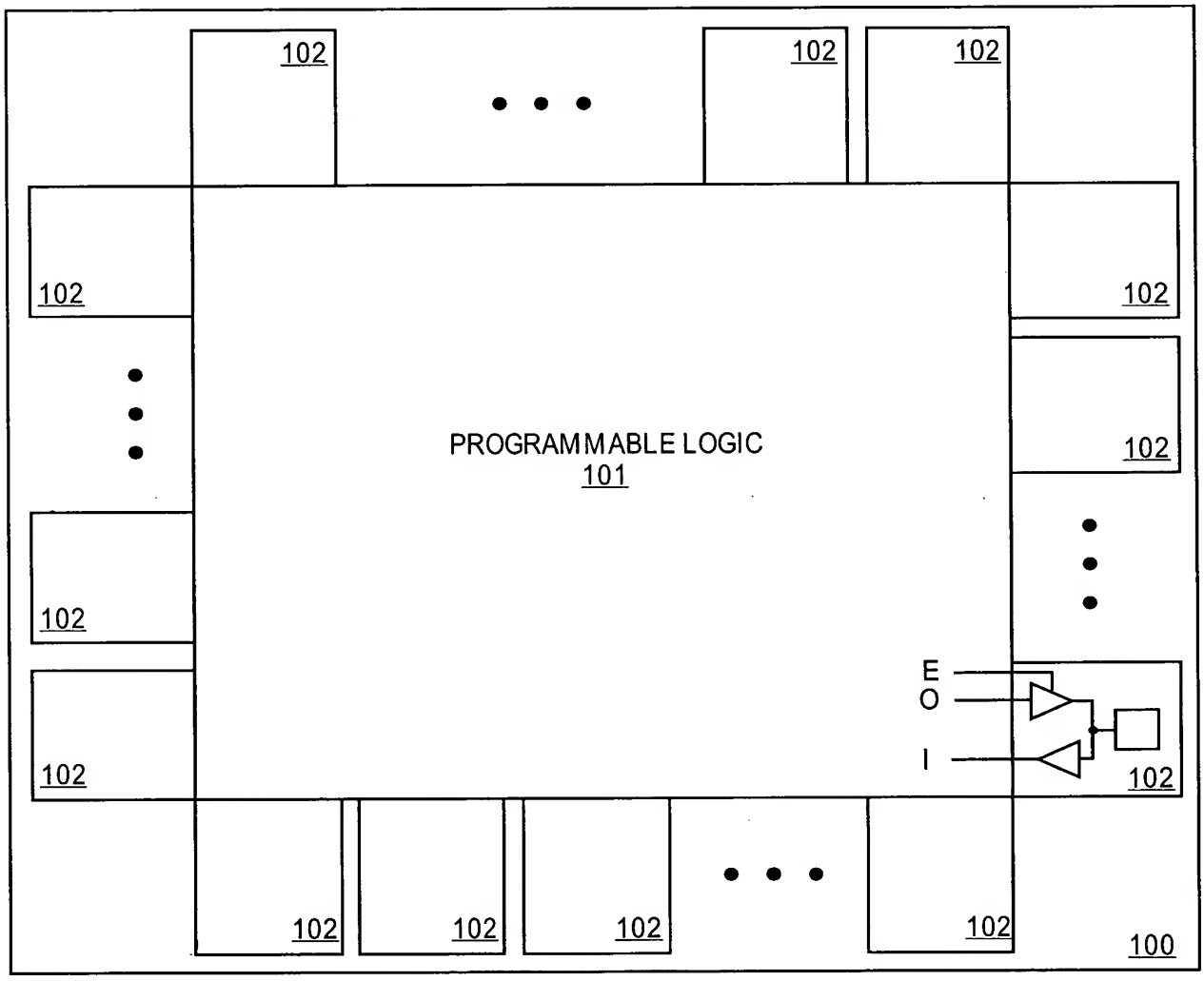

FIG. 1
(PRIOR ART)

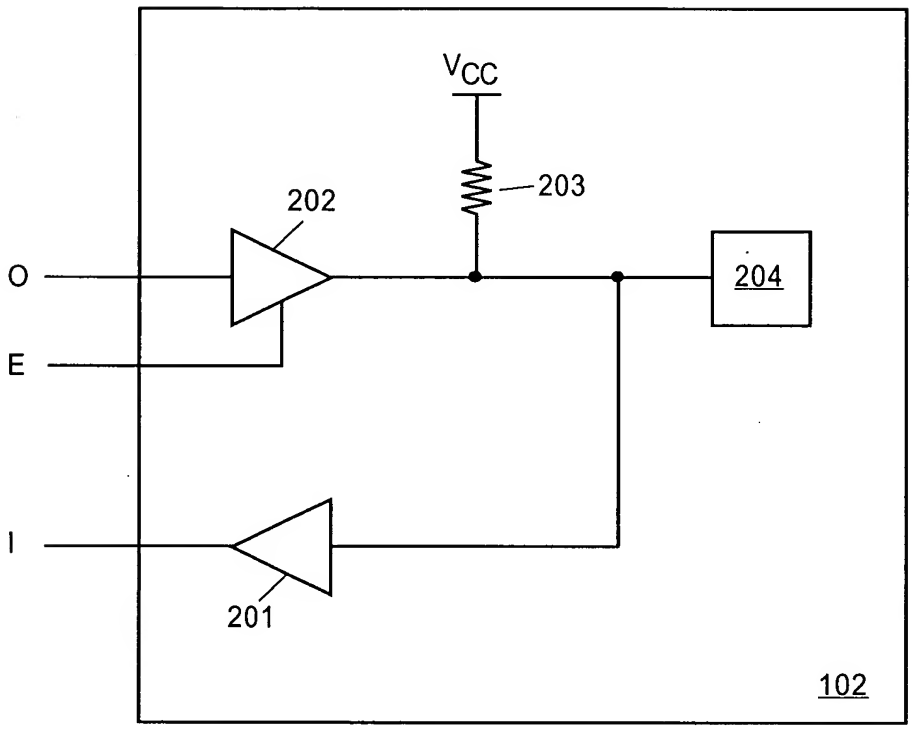

FIG. 2
(PRIOR ART)

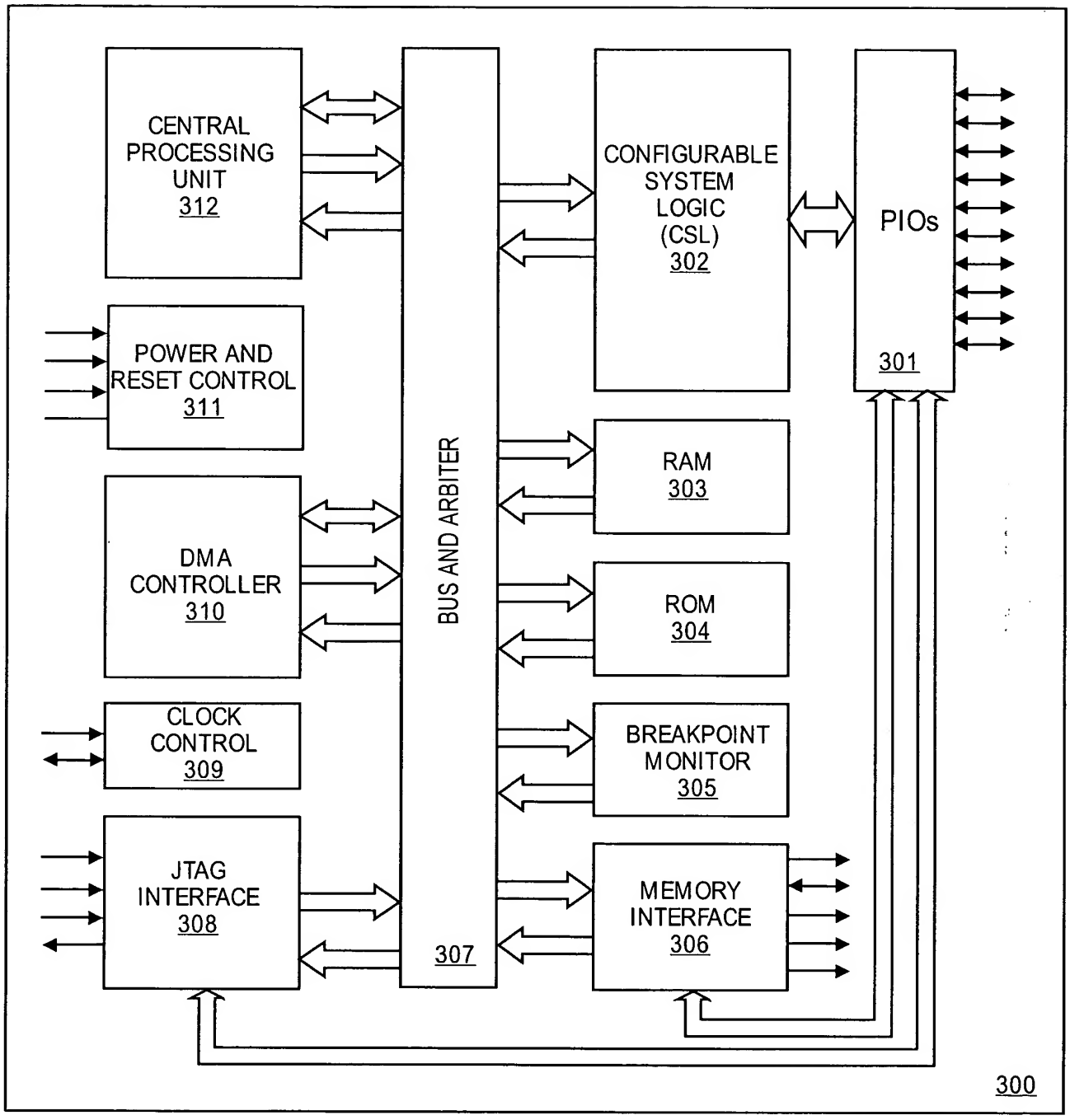
CENTRAL PROCESSING UNIT 312
POWER AND RESET CONTROL 311
DMA CONTROLLER 310
CLOCK CONTROL 309
JTAG INTERFACE 308
BUS AND ARBITER
307
CONFIGURABLE SYSTEM LOGIC (CSL) 302
RAM 303
ROM 304
BREAKPOINT MONITOR 305
MEMORY INTERFACE 306
PIOs
301
300

FIG. 3

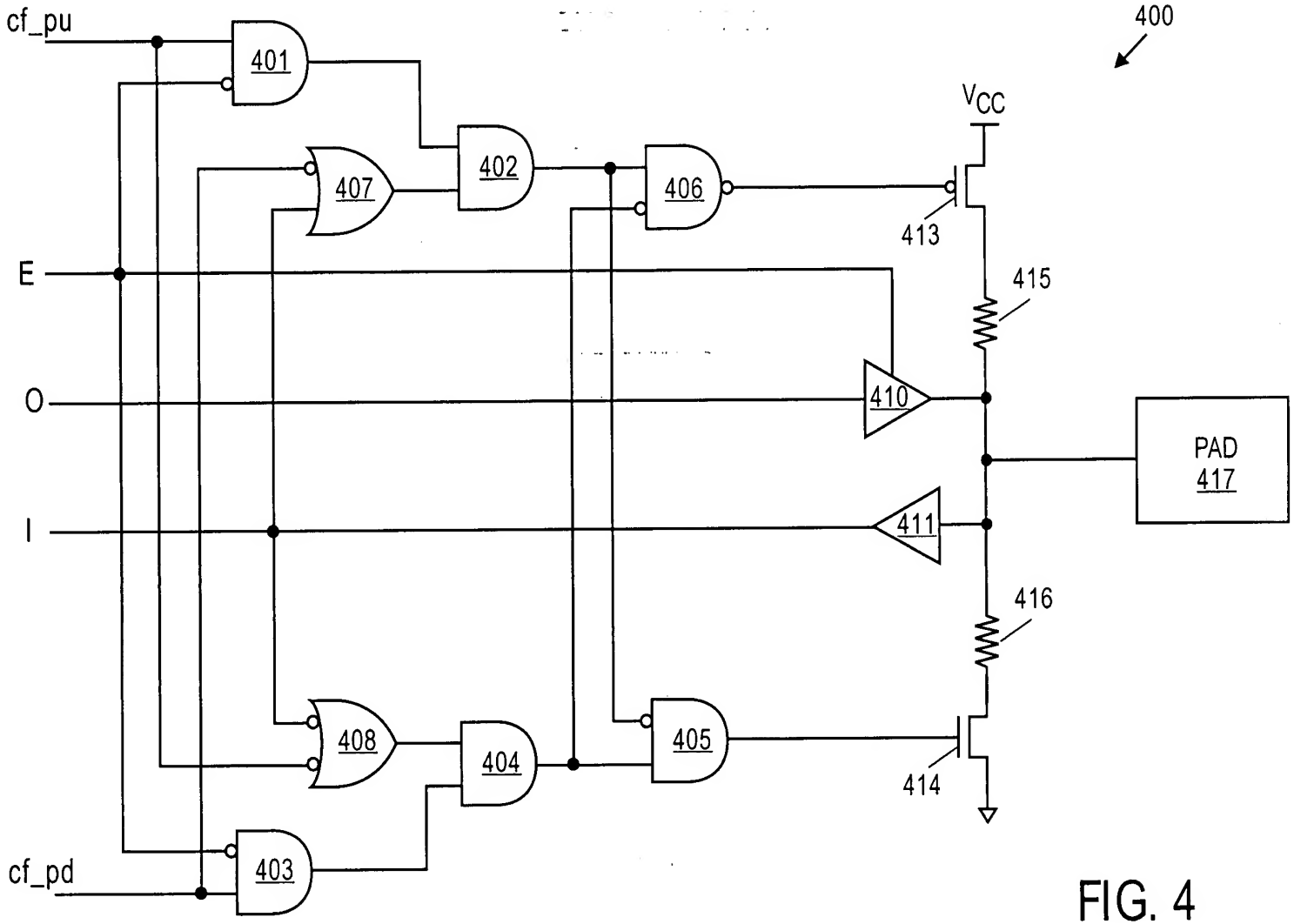
cf_pu
401
400
V_{CC}
407
402
406
413
E
415
O
410
PAD
417
I
411
416
408
404
405
414
cf_pd
403

FIG. 4

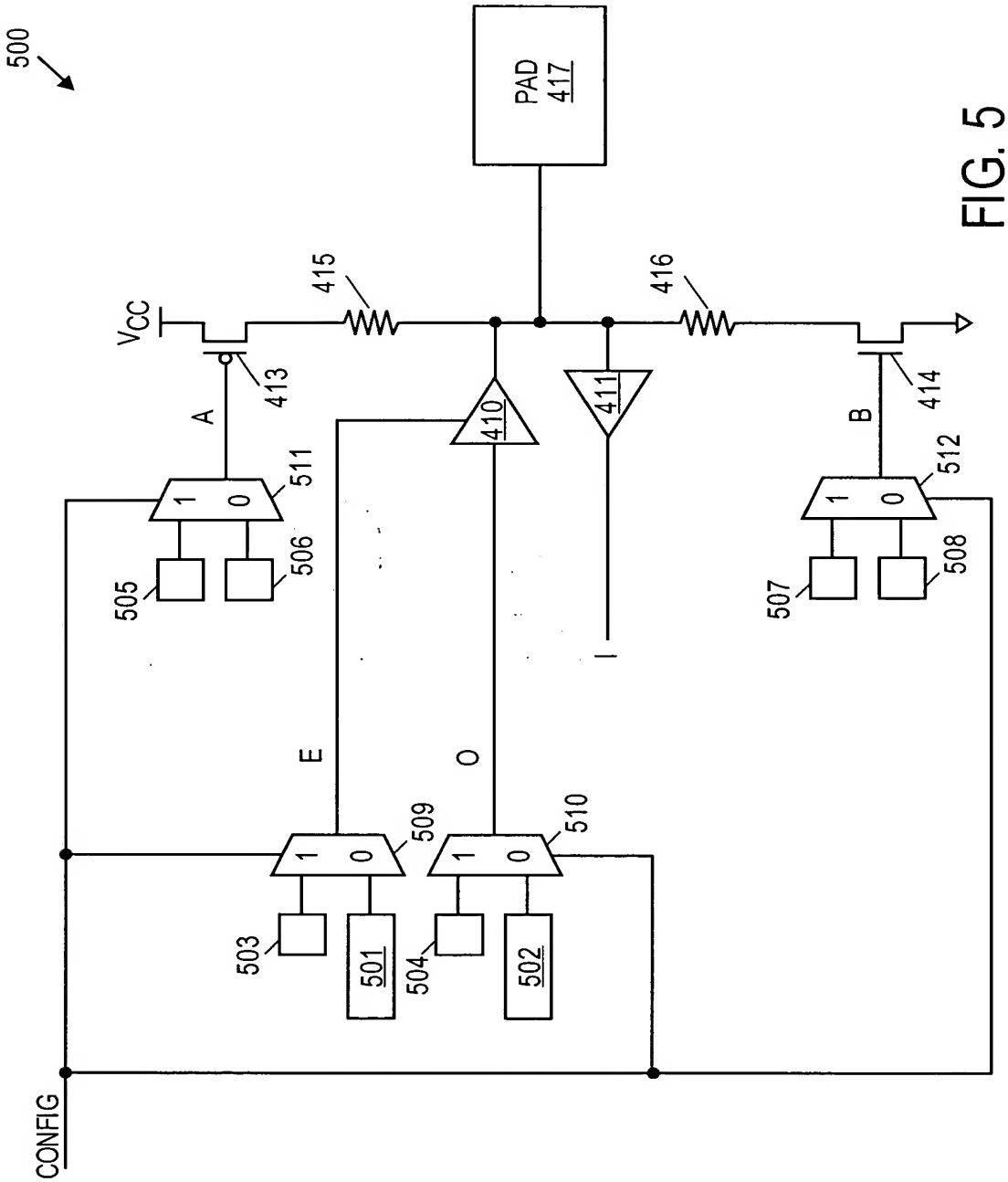
500
PAD
417
VCC
415
416
413
414
410
411
A
B
E
O
I
511
512
505
506
507
508
509
510
503
501
504
502
CONFIG
1
0

FIG. 5

CONFIG = 0

User Output Enable Logic 501	Memory Cell 506	Memory Cell 508	I/O Pad 417
0	0	0	Weak pull-up
0	0	1	Invalid State
0	1	0	No Mode Active
0	1	1	Weak pull-down
1	0	0	User Output Data Logic 502 plus weak pull-up
1	0	1	Invalid State
1	1	0	User Output Data Logic 502
1	1	1	User Output Data Logic 502 plus weak pull-down

FIG. 5A

CONFIG = 1

Memory Cell 503	Memory Cell 505	Memory Cell 507	I/O Pad 417
0	0	0	Weak pull-up
0	0	1	Invalid State
0	1	0	No Mode Active
0	1	1	Weak pull-down
1	0	0	Invalid State
1	0	1	Invalid State
1	1	0	Strongly driven to User Output Data Logic 502
1	1	1	Invalid State

FIG. 5B

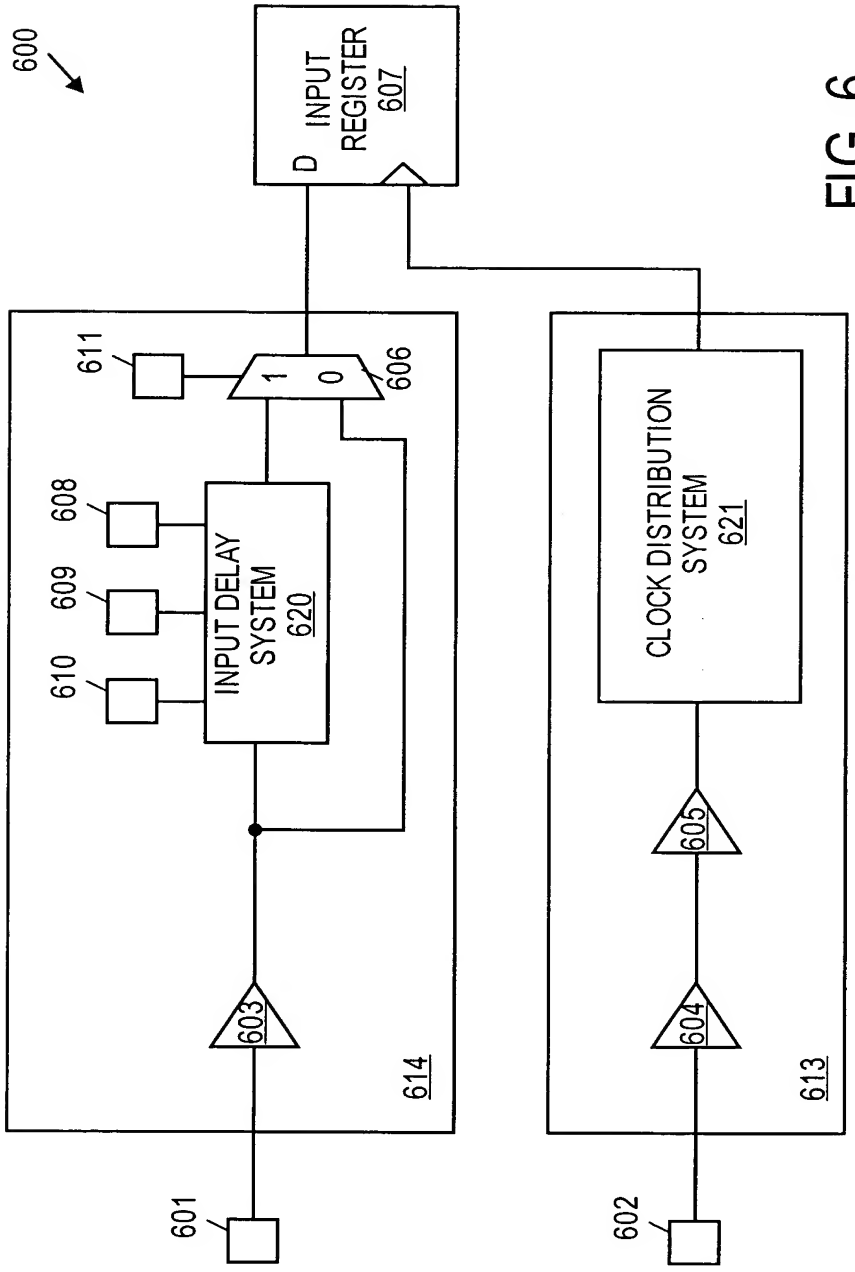
600
D INPUT REGISTER 607
611
1
0
606
608
609
610
INPUT DELAY SYSTEM 620
603
614
601
CLOCK DISTRIBUTION SYSTEM 621
605
604
613
602

FIG. 6

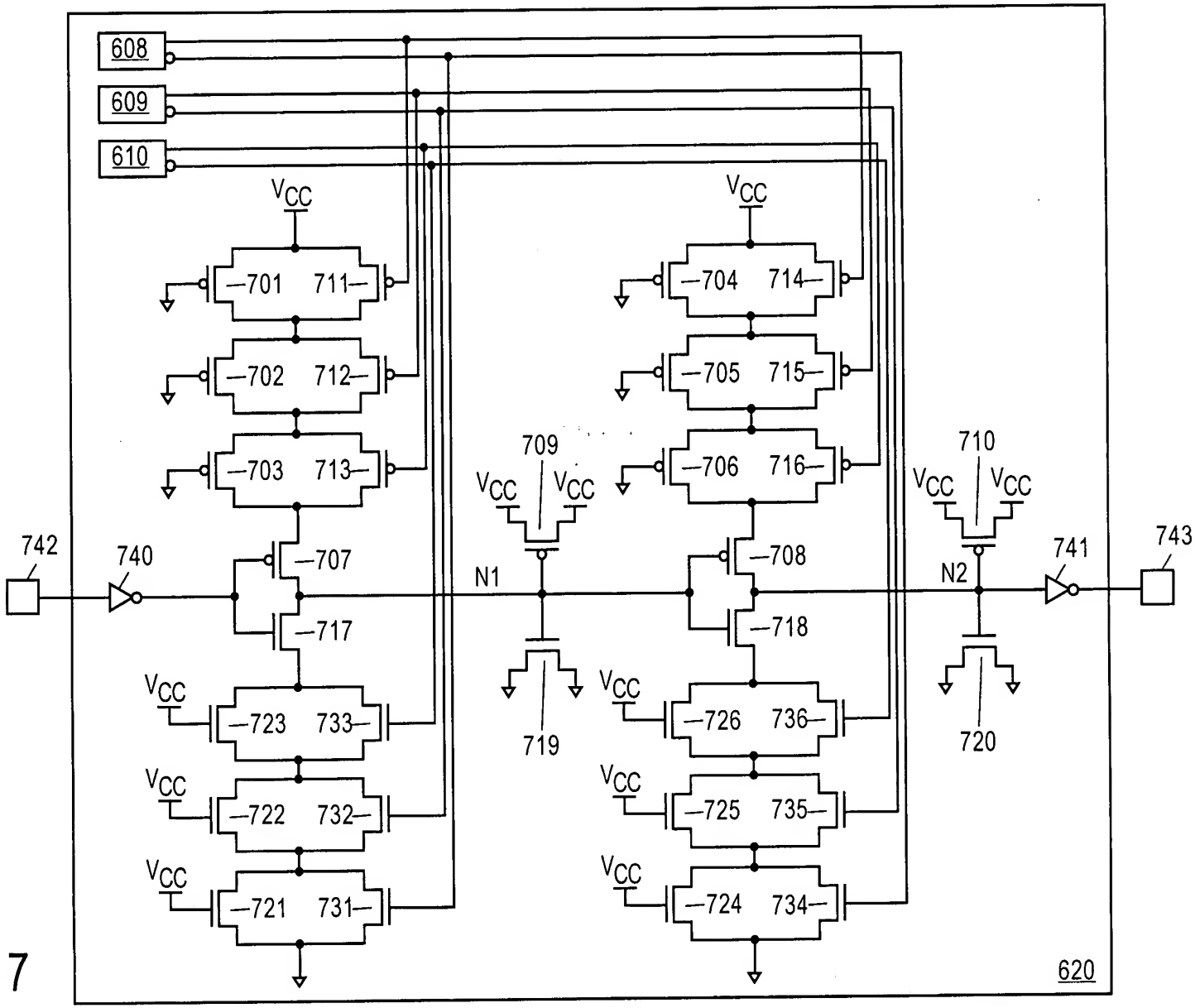
608
609
610
V_{CC}
701
711
702
712
703
713
704
714
705
715
706
716
707
717
708
718
709
710
742
740
N1
N2
741
743
719
720
723
733
722
732
721
731
726
736
725
735
724
734
620

FIG. 7

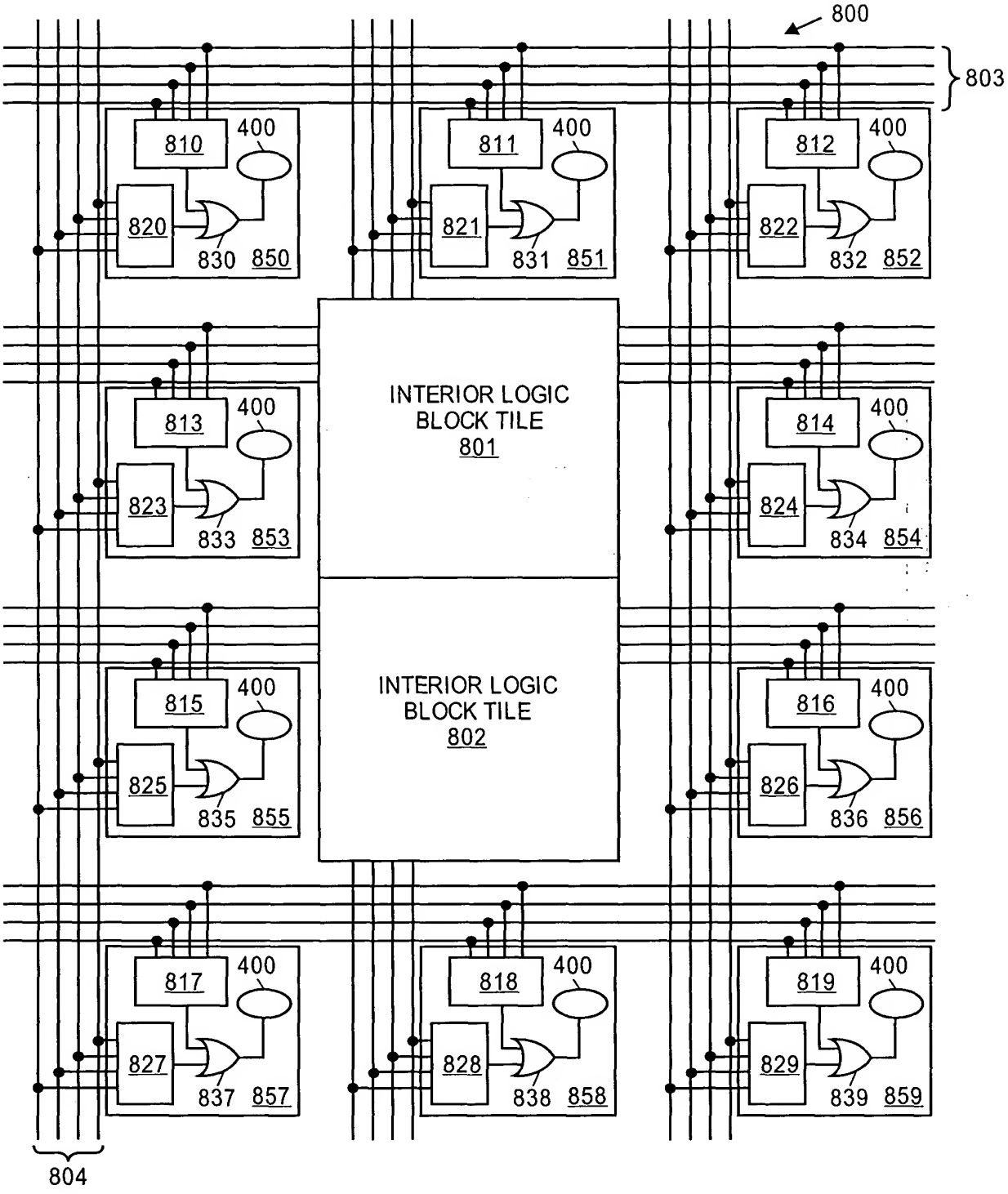
800
803
804
810
400
820
830
850
811
400
821
831
851
812
400
822
832
852
813
400
823
833
853
INTERIOR LOGIC BLOCK TILE 801
814
400
824
834
854
815
400
825
835
855
INTERIOR LOGIC BLOCK TILE 802
816
400
826
836
856
817
400
827
837
857
818
400
828
838
858
819
400
829
839
859

FIG. 8A

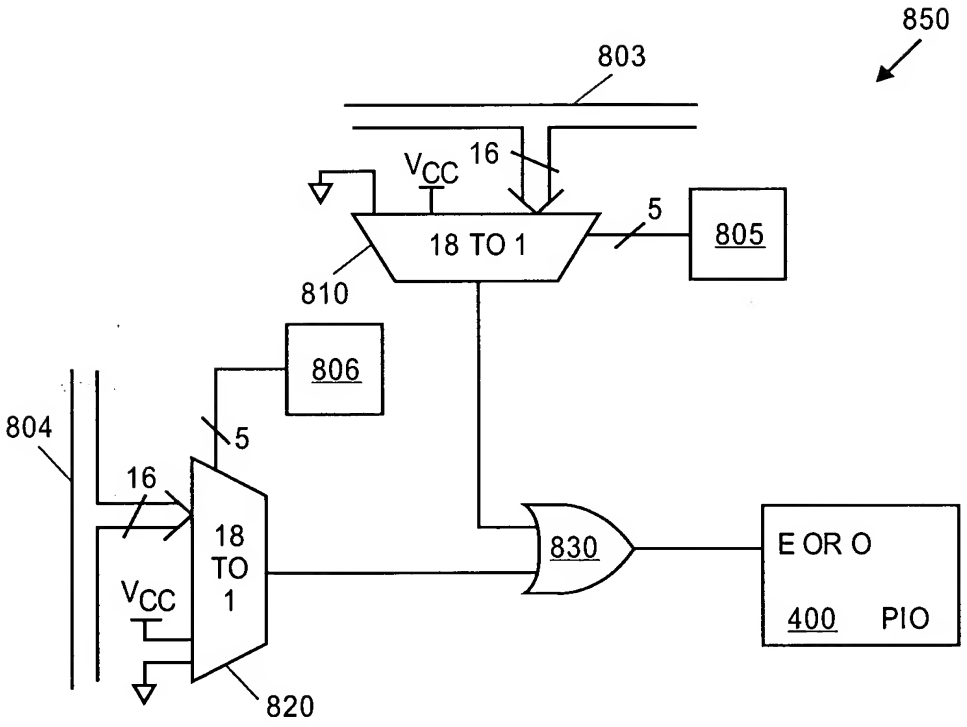
850
803
V_{CC}
16
18 TO 1
5
805
810
806
804
5
16
18
TO
1
V_{CC}
820
830
E OR O
400
PIO

FIG. 8B

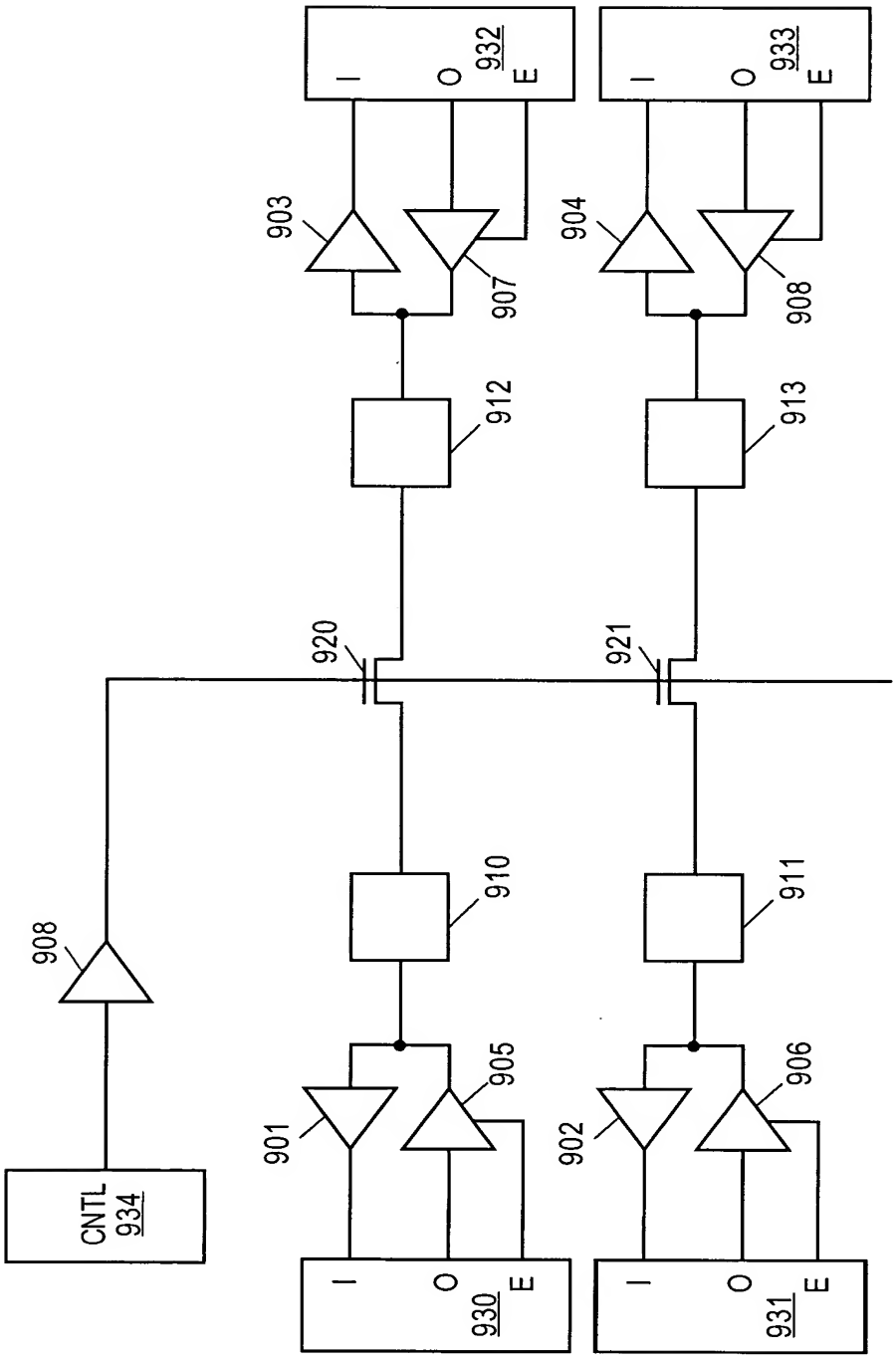
CNTL
934
908
901
905
902
906
930
931
I
O
E
910
911
912
913
920
921
903
907
904
908
932
933

FIG. 9

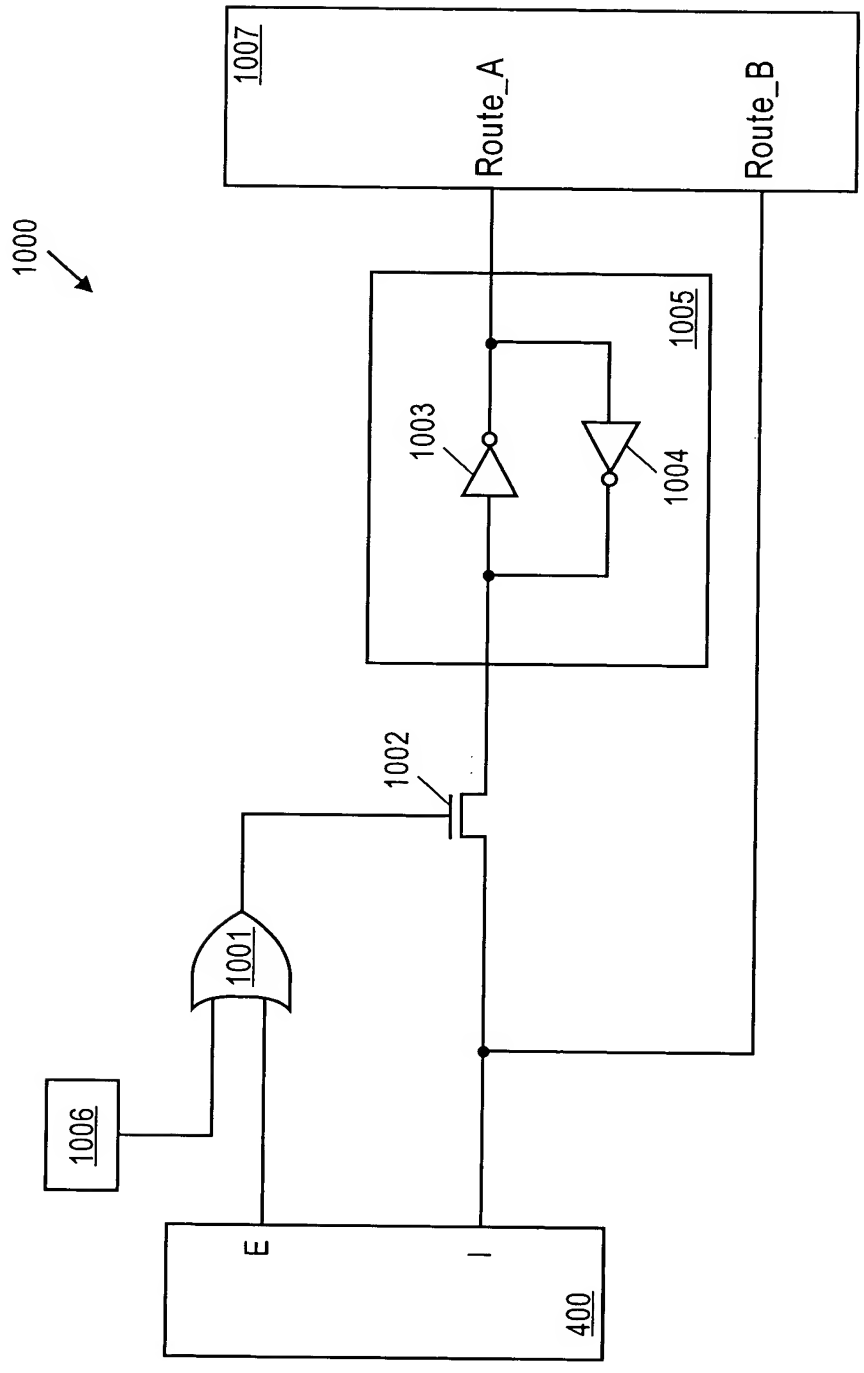

FIG. 10